

# 40-Gbit/s D-type Flip-Flop and Multiplexer Circuits Using InP HEMT

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## ABSTRACT

We developed a novel design technique for a D-type flip-flop (D-FF) circuit that is based on a small-signal-equivalent circuit approach. This technique provides the best condition to operate the D-FF at a high frequency. Using this technique, we fabricated a Master-Slave D-FF using a 0.15- $\mu$ m InP HEMT technology. We achieved 40-Gbit/s operation with clear-eye-waveform patterns and reduced jitter.

## INTRODUCTION

The rapid growth of the Internet and the emergence of web-based multimedia communication have created the need for the backbone optical networks to have a much larger transmitting capacity. Therefore, the development of a 40-Gbit/s time-division multiplexing transmission (TDMA) system is ongoing [1]. The D-type flip-flop (D-FF) is one of the key digital circuits for realizing a TDMA system. Several D-FFs have been proposed, and their performance has been reported to be good [2-3]. However, it has not been clear how to go about finding the optimal condition that provides the best performance. Therefore, we developed a design technique for a D-FF that is based on a small-signal-equivalent circuit approach. We demonstrated its effectiveness by fabricating a D-FF and MUX IC using a 0.15- $\mu$ m InP HEMT.

## CIRCUIT DESIGN TECHNIQUE

A source-coupled FET logic (SCFL) type D-FF circuit consists of two D-latches, as shown in Fig. 1. The switching speed of this circuit can become more than 40 Gbit/s by optimizing the gate-width size of the FET.

Figure 2 shows the simulated output waveform of a D-FF. The data is a pseudo random bit sequence (PRBS) with  $2^7-1$  at 40 Gbit/s. The waveform of a conventional D-FF with the same gate-width has an upstairs pattern near the high state (Fig. 2(a)).

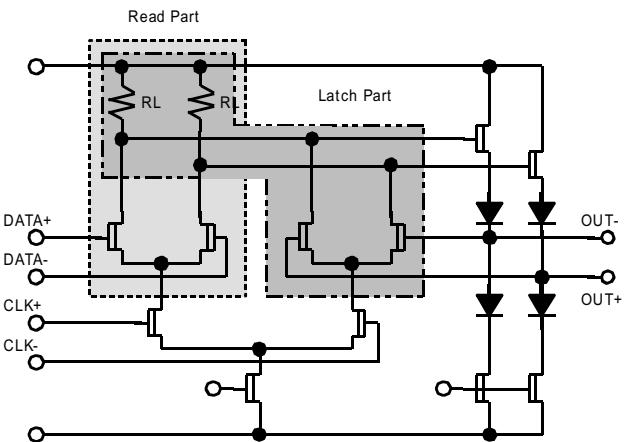
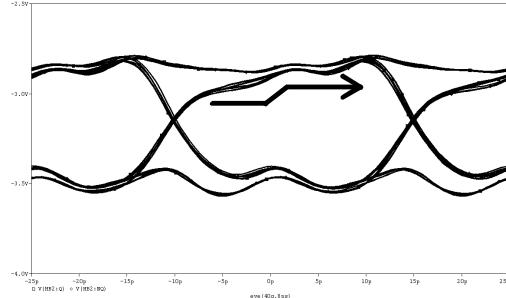
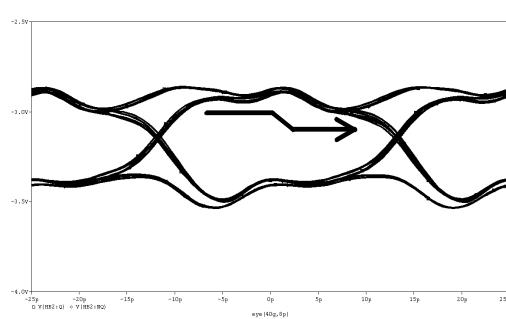


Fig. 1 Schematic of D-latch



(a) Conventional

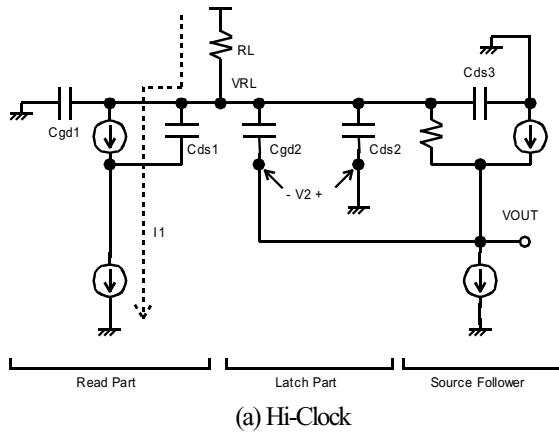


(b) A half-size of the gate-widths for latch

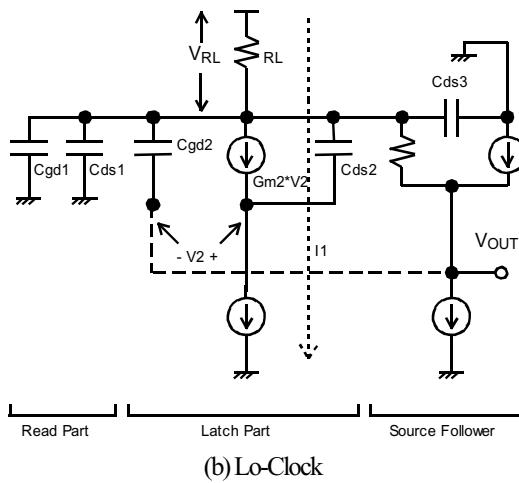
Fig. 2 Simulated results of output waveform of a D-FF

However, when we apply a half-size of the gate-widths to the latch part, the waveform becomes a downstairs shape (Fig. 2(b)). To find the optimum relationship of the gate-widths of the FET between the read part and latch parts, we performed a small-signal-equivalent circuit analysis. To substitute small-signal conditions for large-signal responses, we divided the problem into two clock levels.

Figure 3 shows the small-signal-equivalent circuit of the D-latch. Variations of voltage at OUT ( $V_{OUT}$ ) will be nearly equal to that of voltage at the node of  $R_L$  ( $V_{RL}$ ) when we neglect the voltage losses of the source followers. To simplify the analysis, we implemented our small-signal analysis with  $V_{RL}$ .



(a) Hi-Clock



(b) Lo-Clock

Fig. 3 Small-signal-equivalent circuit of D-latch

#### 1) Hi-clock level (Fig. 3(a))

When the clock becomes hi-level, current  $I_1$  changes its path toward the read part, and  $V_{RL}$  is changed. The CR time constant of  $V_{RL}$  ( $\tau_H$ ) determines the switching speed of the D-latch, and is

expressed as follows;

$$\tau_H = R_L (C_{gd1} + C_{ds1} + 2C_{gd2} + C_{ds2} + C_{gd3}) . \quad (1)$$

The capacitance  $C_{gd2}$  has a factor of two due to positive feedback from the latch-part.  $V_{RL}$  is given by;

$$V_{RL}(t) = R_L I_1 (1 - \exp(-t / \tau_H)) . \quad (2)$$

As shown in Equation (2), although it is preferable that  $\tau_H$  is small, we cannot reduce the gate-width of FETs in the read part since the voltage gain needs to be more than one. The gate-widths of the source-follower cannot be reduced either, since it has to maintain driving force capabilities for the circuits that follow.

#### 2) Lo-clock level (Fig. 3(b))

When the clock becomes lo-level, current  $I_1$  changes its path toward the latch part. Also,  $V_{RL}$  changes from that of when the clock is hi-level ( $V_\alpha$ ). If  $V_\alpha$  is equal to  $R_L I_1$ ,  $V_{RL}$  is not changed because the data signal is maintained at the latch part. In such a condition,  $V_{RL}$  are given by,

$$V_{RL} = R_L I_1 . \quad (3)$$

However,  $V_\alpha$  is not equal to  $R_L I_1$ ;  $V_{RL}$  is changed from  $V_\alpha$ .

The CR time constants of  $V_{RL}$  ( $\tau_L$ ) and  $V_{RL}$  are expressed as:

$$\tau_L = \frac{R_L}{1 - G_{m2}R_L} (C_{gd1} + C_{ds1} + 2C_{gd2} + C_{ds2} + C_{gd3}) . \quad (4)$$

$$V_{RL}(t) = V_\alpha \exp(-t / \tau_L) \quad (5)$$

Equation (4) includes a factor of  $G_{m2}$  due to positive feedback from the latch-part. When the  $G_{m2}R_L$  is larger than one,  $V_{RL}$  grow large rapidly to  $R_L I_1$ . On the other hand, when  $G_{m2}R_L$  is smaller than one,  $V_{RL}$  becomes smaller than  $V_\alpha$ . This indicates that the latch part cannot maintain the data.

Figure 4 shows relationships between  $V_H$ ,  $V_L$ , and the gate-width ratio of the latch part to the read part. Here,  $V_H$  and  $V_L$  are normalized  $V_{RL}$  by  $R_L I_1$ .  $V_H$  is the value when the clock level is high,  $V_L$  is that of when clock level is low. In our calculations, we defined the  $V_H$  and  $V_L$  as values at 7 psec that were derived from the cutoff-frequency ( $f_T$ ) of our InP HEMT. This graph indicates that the conventional D-FF with a gate-width ratio of one, has an upstairs shaped waveform because  $V_H$  is smaller than  $V_L$ . As for the case of a small sized FETs used for the latch, the waveform had a downstairs shape.

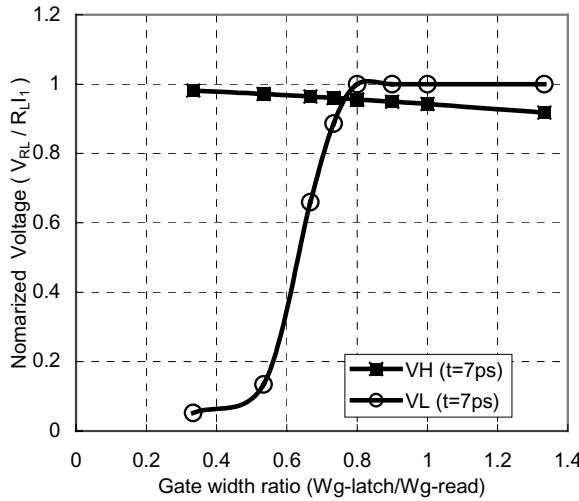


Fig. 4 Calculated voltage of the D-latch

To improve the waveform into an ideal rectangular shape, it is necessary that  $V_H$  be equal to  $V_L$ . From the figure and the above discussion, we can find the optimum gate-width ratio that provides the best performance for a D-FF. We obtained the ratio of 0.8 for our FETs. To verify the accuracy of our design method, we designed and fabricated a D-FF circuit with our 0.15- $\mu$ m InP HEMT technology. The gate-width ratio was set to be 0.8.

## EXPERIMENTAL RESULTS

Figure 5 shows a block diagram of the D-FF and MUX ICs.

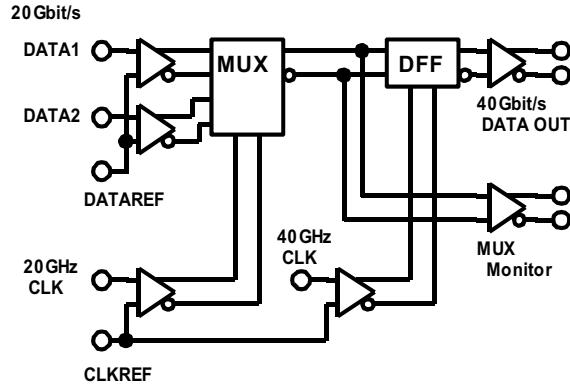


Fig. 5 Circuit block diagram

There are a single data input and a differential data output that are connected to a 50-ohm termination. In front of the MUX and D-FF cores, data and clock buffers are located to convert the single-phase

signal to a differential signal. A pair of two-channel input data was multiplexed at the MUX. The multiplexed data was clocked at the D-FF circuit. The supply voltage was -5.2 V. The power consumption was 2.5 W. A micrograph of the chips is shown in Fig. 6. The total chip area was  $2.4 \times 1.9$  mm<sup>2</sup>.

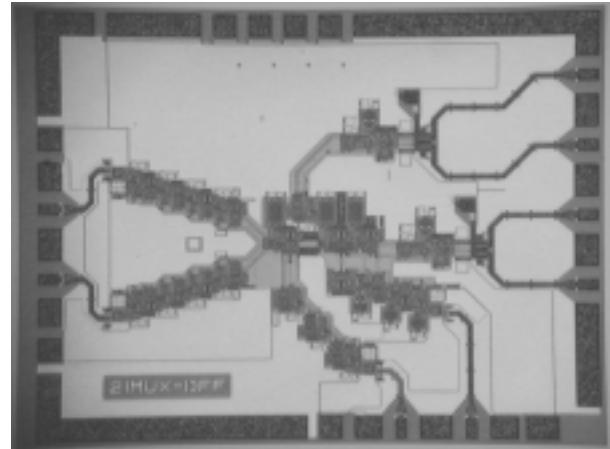
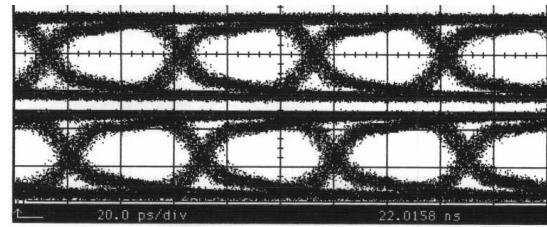
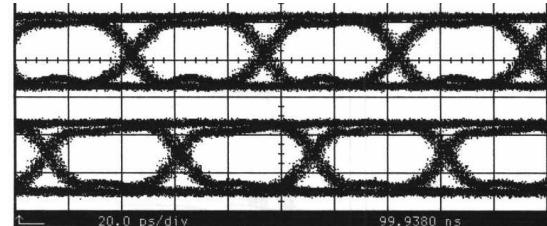


Fig. 6 Micrograph of the ICs

Figure 7 shows the output eye patterns at 20 Gbit/s. The conventional D-FF had steps and it could not be operated at 40 Gbit/s. On the other hand, the improved D-FF had a very clear waveform.



(a) Conventional D-FF



(b) Improved D-FF

Fig. 7 Output waveform at 20 Gbit/s

Figure 8 shows the output eye waveform of the MUX at 40 Gbit/s. Figure 9 shows those of the improved D-FF at 40 Gbit/s. The output data of the D-FF circuits had decreased jitter and very clear eye waveform. This result indicates that the small-signal-equivalent circuit analysis was effective.

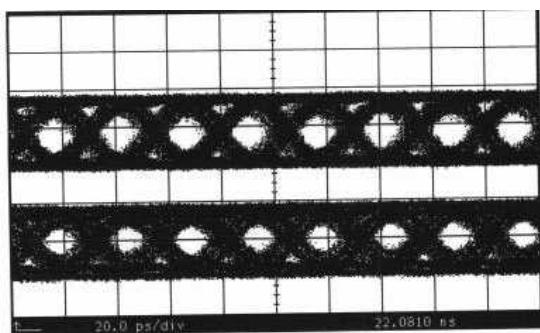


Fig. 8 Output waveform of MUX at 40 Gbit/s

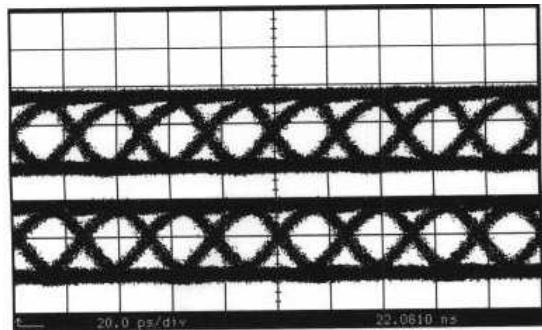


Fig. 9 Output waveform of improved D-FF at 40 Gbit/s

## CONCLUSION

We developed a novel small-signal design technique to improve the waveform of D-FF circuits operated at high frequencies. We have applied the technique to D-FF and MUX circuits using a 0.15- $\mu$ m InP HEMT. This IC operated at 40 Gbit/s, and the eye waveform was very clear. Our design technique is very convenient and useful for designing any type of D-FF circuit.

## REFERENCES

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